Using EPC Space Products to Design a Low Parts Count Implementation of an Active-Clamp, Synchronously-Rectified Forward Converter

Space-based power supply applications require both high-efficiency power conversion and high reliability from the circuit. Sometimes these two goals are at odds with one-another and there are tradeoffs that must be made between the two for a chosen conversion topology.

The synchronously-rectified, active-clamp variant of the forward converter topology offers the space system circuit designer a much-improved alternative to the standard version of this converter type. But before the improved version is considered, a short discussion of the benefits and shortfalls of the forward converter is in order.

An efficient step-down conversion topology often selected for space power applications is the isolated forward converter, shown in Figure 1. This converter type is a member of the step-down, or buck, converter family. The output voltage for this converter is: $V_{OUT} = V_{DD} \cdot (N_S/N_P) \cdot D$, where N_S are the secondary turns on the transformer, N_P are the primary turns and D is the operating duty cycle.

Depending upon the elements selected for SW1, D1 and D2 the conversion efficiency for the circuit in Figure 1 can be acceptably high, in the 80-85% range, depending upon the output voltage required. Lower output voltages – lower duty cycles – always yield lower conversion efficiencies because for a given fixed output current, the output power ($P_{OUT} = V_{OUT} \cdot I_{OUT}$) decreases and the power losses due to the components become a larger part of the total power conversion efficiency ($\eta = P_{OUT} / P_{IN}$, where $P_{IN} = P_{OUT} + P_{losses}$). For the circuit shown in Figure 1, the majority of the power losses occur in rectifier diodes D1 and D2, the primary power switch SW1 and the power/isolation transformer T1.

The conversion efficiency of the basic forward converter may be increased significantly, to 90% and above, by employing the secondary-side rectification technique known as synchronous rectification, as shown in Figure 2. In this method, the two diodes (D1 and D2 in Figure 1) are replaced with low $R_{DS(on)}$ power switches whose ON/OFF states are synchronized with the ON state of the primary power switch.

In Figure 2 the two added power switches SW2 and SW3 perform the exact same function as diodes D2 and D3 in Figure 1. The circuit becomes slightly more complex as additional PWM clocking and switching signal galvanic isolation must be added to ensure that SW1 and SW2 are ON simultaneously and SW3 is OFF when either SW1 or SW2 are ON. Also, "dead" times must be added to account for the switching delays of all the power switches to prevent unwanted switch ON-state overlaps. For a synchronous forward converter as depicted in Figure 2, conversion efficiencies in the range of 90-96% are possible.

A very important consideration when implementing the forward converter topology is that the switching node voltage excursion(s) during operation must be carefully determined and accounted for when selecting the power switches in the circuit. When the primary winding of the power transformer is energized (when the primary power switch SW1 is ON) it stores energy in proportion to the Volt-seconds applied to that winding. When the power switch turns OFF, that energy is released into a high impedance and the resultant voltage at the switching node (SN) will attain a very high level above V_{DD}, ultimately breaking down and destroying the power switch from the energy released. To prevent this destruction,

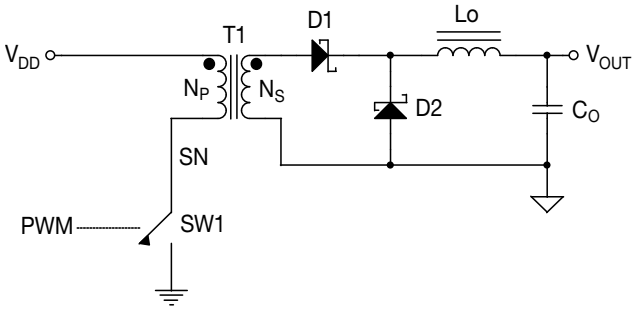


Figure 1: The Basic Isolated Forward Converter

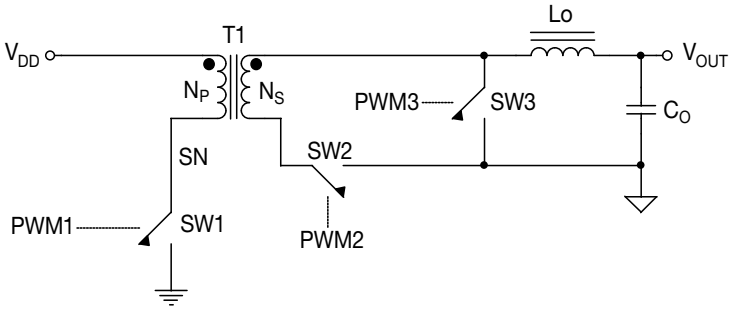
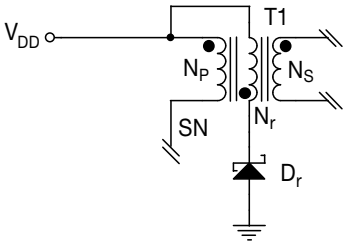


Figure 2: The Synchronously-Rectified Isolated Forward Converter

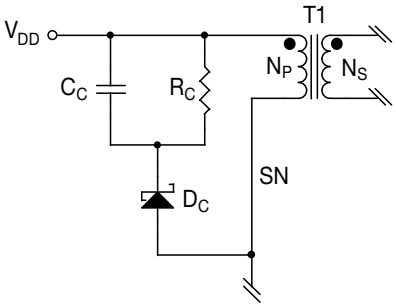
a protective countermeasure is required to "constrain" the voltage level during the reset event, along with the voltage spike that results from the energy released in the power transformer's primary leakage inductance.

Frequently as good design practice, to constrain the voltage excursions at the SN, the designer will opt to place a tertiary/reset winding on the power transformer or to add an RCD reset network across the primary winding (see Figure 3). Both of these techniques clamp the SN voltage to a predictable value and then return the energy required to reset the core to the V_{DD} power supply (as well as the energy stored in the leakage inductor), but at a cost – complexity, added components and added power loss.

The major design challenge with the forward converter is to observe de-rating guidelines for voltage stress for the primary power switch: The circuit must be carefully designed to account for the voltage excursions at the switching node AND the primary power switch MUST be carefully chosen for drain-source breakdown voltage in the conventional, unconstrained forward converter topology. This often leads to a Hobson's choice trade-off between the reset method chosen, component ratings, and efficiency. But what if this situation, this difficult choice, became less of a consideration, and the voltage at the switching node could be closely constrained and controlled in a simple, effective manner?



Tertiary Reset Winding



RCD Clamp

Figure 3: Conventional Forward Converter Transformer Reset Techniques

Enter the Active-Clamp Forward Converter (ACFC)!

A variant of the synchronous forward converter, there are two forms of the ACFC – the low-side or grounded switch version, shown in Figure 4 and the high-side or SN-referenced switch version shown in Figure 5. For purpose of this discussion we will consider the high-side version of the ACFC, which employs an n-channel clamp switch in the following discussion.

Please note that for proper operation that the clamp switch SW4 in the high-side ACFC requires a floating/isolated gate drive signal to the switch.

A benefit of the ACFC is that Volt-second (V-t) balance is achieved in the transformer's primary and the reset energies in the transformer primary and the leakage inductance are "recycled" with little loss back to V_{DD} as an inherent function of its operation. In the circuit in Figure 5, the voltage across the clamp capacitor is that of a buck-boost converter whose duty cycle is locked to that of the main power switch, SW1. At any duty cycle, the voltage across the clamp capacitor is $V(C_{clamp}) = V_{DD} \cdot (D / (1-D))$, where D is the duty cycle of SW1. For example, if V_{DD} = 50 V and D = 0.5 (50%), the clamp voltage is $V_{DD} \cdot (0.5 / 0.5)$ or 50 V. Thus, the voltage at the switching node is $V_{DD} + V(C_{clamp})$ = 50 V + 50 V = 100 V. This makes intuitive sense as at 50% duty cycle the ON and reset V-t products are equal, so the voltage at the switching node must be 100 V (50 V above the V_{DD} potential of 50 V) to reset the transformer.

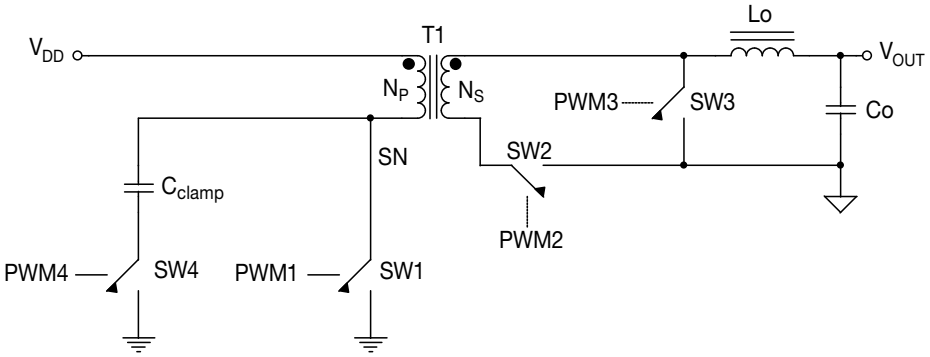


Figure 4: Synchronously-Rectified Low-Side ACFC

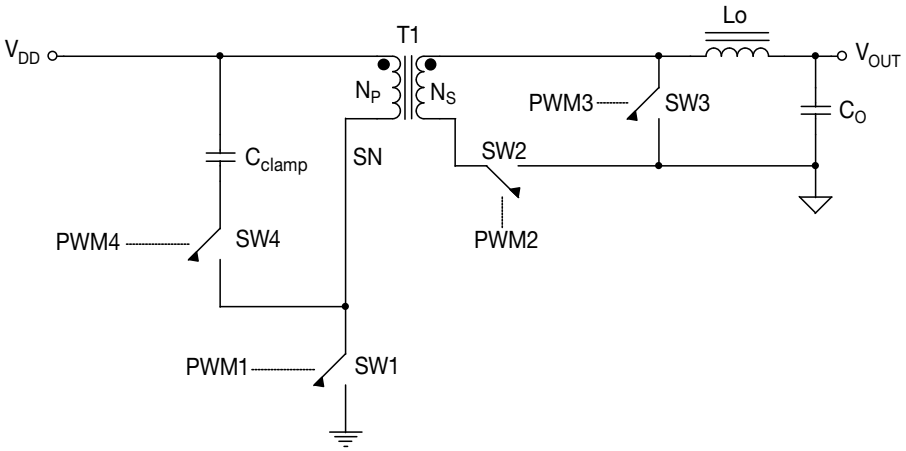


Figure 5: Synchronously-Rectified High-Side ACFC

Figure 6 shows the graph of the voltage variations that can be expected at the switching node (SN) from power switch duty cycles at several different values of V_{DD} for an ACFC. The dashed red line indicates the 50% de-rating point for a power switched rated for 100 V breakdown and the solid red line indicates the 50% de-rating point for a 200 V-rated switch. It should be noted that for the several V_{DD} power supply levels shown in Figure 6 that the maximum duty cycle to meet the deratings is ~30% (0.3). Voltages that exceed the dashed red line cannot be serviced with a 100V device de-rated to 50% operation and voltages that exceed the solid red line similarly cannot be serviced by a 50% de-rated 200 V device.

With its higher efficiency, constrained power switch operating voltage and low parts count, the high-side ACFC the perfect candidate for medium power, space-grade power conversion. EPC Space's product portfolio can easily satisfy this demanding application with a modular, building block approach.

IMPORTANT NOTE: It is not the intent of this design note to detail every aspect of the design of the following ACFC circuit example as the functionality of the circuit and its operation are well-documented in literature. The following design and analysis touches on the salient points of the ACFC with regards to integrating products from the EPC Space portfolio into the circuit shown in Figure 5. The determination of actual component values and modifications to the circuit to suit the actual design requirements of a particular circuit are left to the designer.

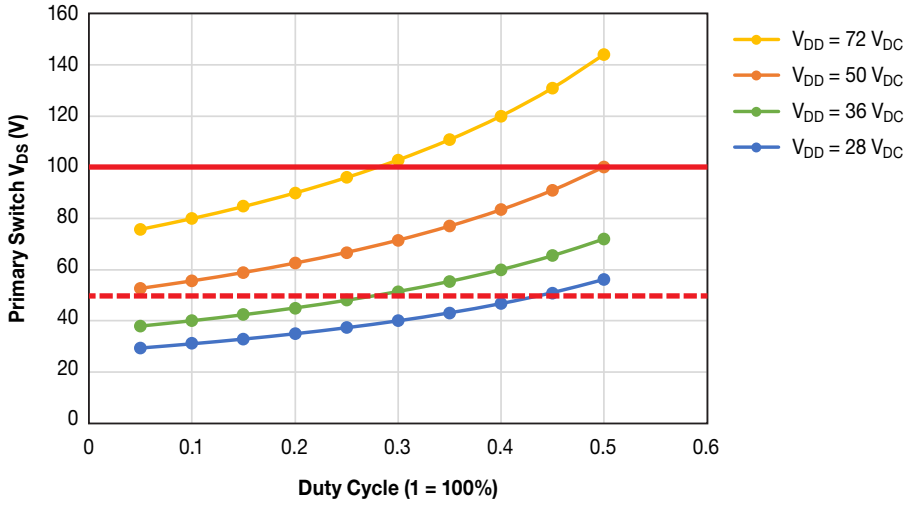


Figure 6: Switching Node (Primary Switch D-S) Voltage as a Function of Duty Cycle

Table I discusses the functionality of each HEMT in the circuit of Figure 5 and the electrical attributes each must possess for each function in the high-side ACFC.

Switch	Function	Voltage	Peak Current	Notes
SW1	Primary Switch	$V_{DD} + V(C_{clamp})$	$DI_{mag} + (I_{OUT} \cdot D / N) + (\Delta I(Lo) / (2 \cdot N))$	(1)(2)(3)(4)
SW2	Secondary Control Switch	$(V_{DD} + V(C_{clamp})) \cdot N$	$(I_{OUT} + (\Delta I(Lo) / 2)) \cdot D$	(2)(4)
SW3	Secondary Synchronous Switch	$V_{DD} \cdot N$	$(I_{OUT} + (\Delta I(Lo) / 2)) \cdot (1 - D)$	(2)(4)
SW4	Clamp Switch	V_{DD}	ΔImag	(2)(4)

Table I. Required Electrical Attributes of the HEMTS in a High-Side ACFC

Note 1: $\Delta Imag = V_{DD} \cdot D / (f_{sw} \cdot D)$

Note 2: $\Delta I(Lo) = (V_{DD} / N - V_{OUT}) \cdot D / (f_{sw} \cdot Lo)$

Note 3: $N = N_S / N_P$

Note 4: The switch function requires an anti-parallel diode/rectifier for proper circuit operation.

In order to better visualize the real-world ACFC implementation, consider Figure 7 where the primitive switches in Figure 5 are replaced with their n-channel HEMT substitutes, along with the requisite anti-parallel Schottky diodes.

Studying Figure 7 for a moment with regards to the EPC Space discrete and modular lineup it becomes clear that Q1 and D1, a low-side switch and catch rectifier, may be replaced by the FBS-GAM01 – a single power HEMT with anti-parallel catch diode with integrated high-speed gate driver, the voltage rating selected obviously depending upon the magnitude of V_{DD} and the operating duty cycle per Figure 6. Similarly, Q2, D2, Q3 and D3, both low-side switches with catch rectifiers, may be replaced with the GAM04 – dual power HEMTs with catch diodes and high-speed gate drivers in a single package. As for Q4 and D4, the use of a GAM01 would be overkill in terms of current-carrying capability (Q4 only carries magnetizing current due to the primary magnetizing inductance which is much less than the reflected secondary load current), and the output capacitance of these drivers would be too large, and affect the resonance characteristics of the resonating L_{mag} - C_{clamp} pair. Consequently, Q4 is the natural place to use an appropriate discrete-packaged HEMT along with a modular gate driver. As such, the FBG10N05 or FBG20N04, again depending upon V_{DD} and operating duty cycle to select the V_{DSS}, are ideal choices for the clamp switch, and each may be driven by the FBS-GAM01-PSE gate driver module. It should be remembered that Q4 requires an anti-parallel catch Schottky rectifier, so an appropriately-rated voltage breakdown device should be similarly chosen. The current rating for D4 should be such that it is adequate for carrying the transformer's primary magnetizing current (I_{mag}).

Realizing that Q4 requires drive signal isolation, it is necessary to select and implement this isolation to the EPC Space HEMT and gate driver combination selected. For the example in this design note, the NVE IL600 series of GMR (giant magneto-resistive) high-speed digital isolators are suggested to be used to provide the requisite drive signal isolation in the final circuit. In fact, so as to equalize the throughput delays to each switching element, a GMR isolator will be used as a front-end for all four of the power switch elements (even though Q1 does not require drive signal isolation – the rest, however do).

The schematic shown in Figure 8 shows the ACFC circuit with the requisite EPC Space devices included and the necessary gate drive and secondary bias power embellishments.

In this solution, secondary 5V bias power for the GAM04 module is derived from the output inductor, L2, "stealing" energy from its core using a second low-power winding. The peak voltage at this secondary is derived from the output voltage and the N_S/N_P windings turns ratio. This voltage will be quasi-regulated as it is a function of V_{OUT}. If the voltage is too high, a series resistor and shunt Zener diode, or even LDO regulator, may be used to provide the necessary bias level for the GAM04.

Primary current monitoring is supplied to the circuit via current transformer T1 and the associated components. This transformer could be, for example, the Pulse TA1005.100NL, a surface mount component with a small PCB footprint. The gain of the current sensing is determined by the turns ratio of transformer T1 and resistor R6, and is set to 0.1 V/A in the example. This signal could be fed directly to a legacy PWM controller's "CS" (current sense) pin or to the A/D input of a multifunction FPGA, gate array or microcontroller.

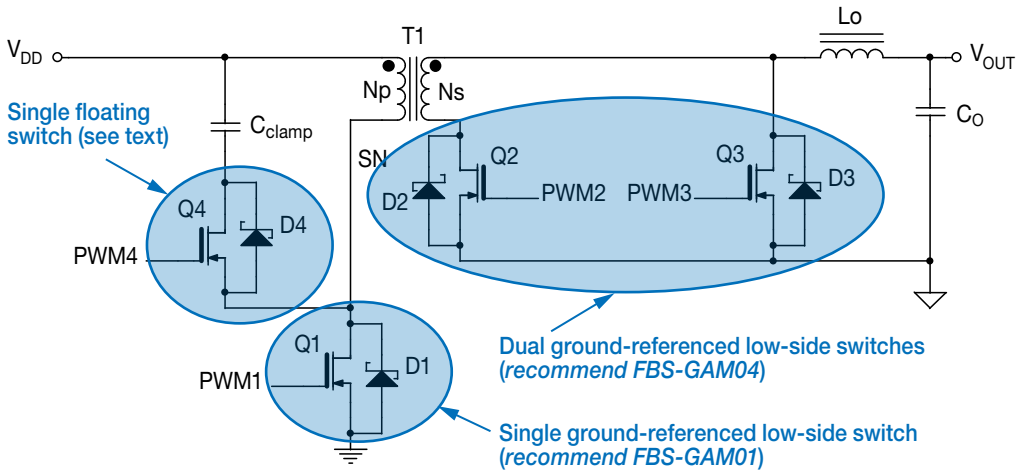


Figure 7. Synchronously-Rectified High-Side ACFC w/HEMTs and Diodes

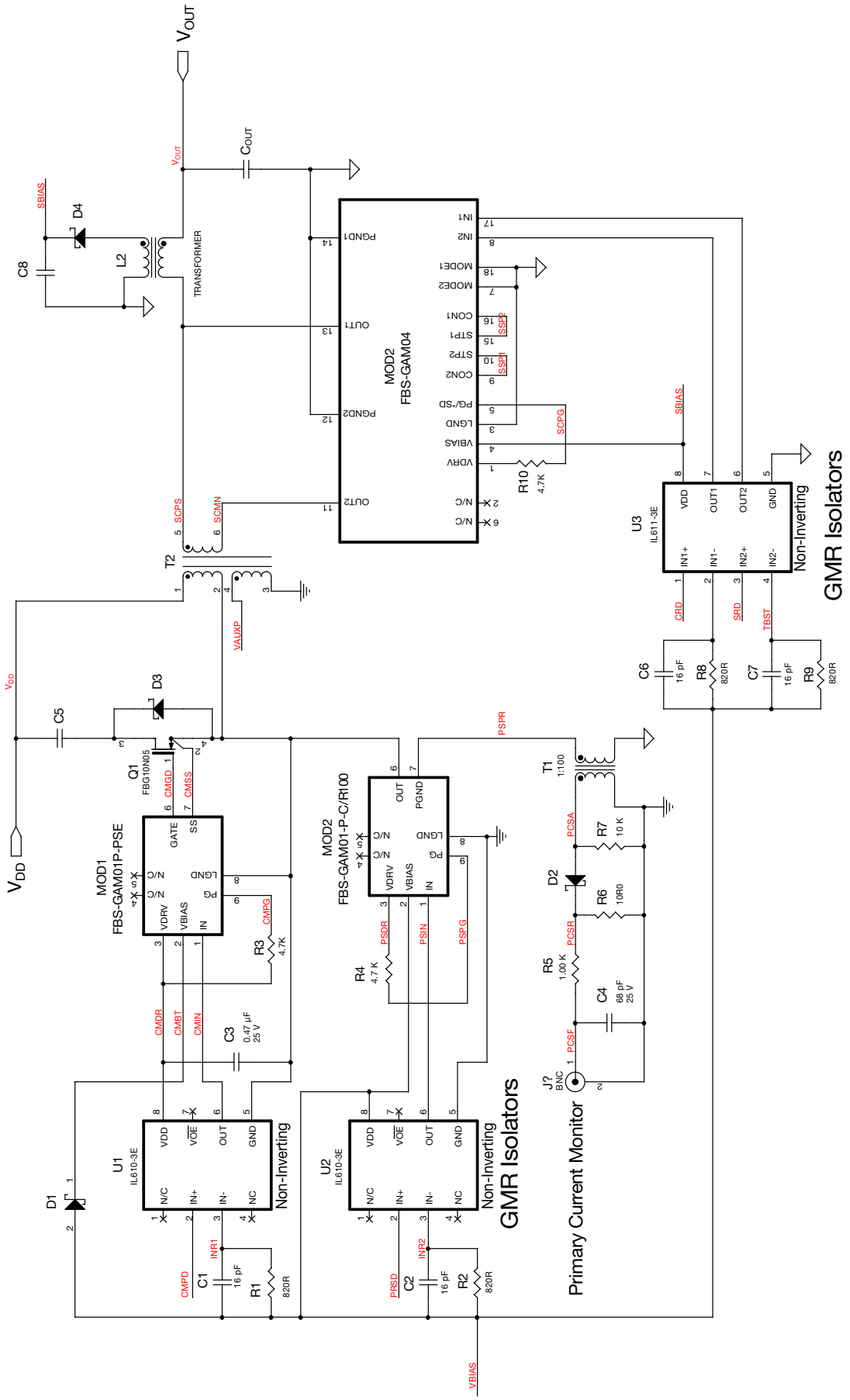


Figure 8. ACFC Complete Schematic with EPC Space Components as Power Switches

Simple primary biasing circuitry to provide the necessary 5 V bias power is shown in Figure 9. This primary bias uses a transient voltage source (D5, D6, D7, C9 and R11) derived from the input voltage V_{DD} to provide the requisite start up energy for the circuit until the converter enters regulation. After that time energy is supplied by the auxiliary winding (Naux) on the power transformer, T1, using D9, D10, D11, L1, C10 and R12. By selecting the two Zener diodes, D6 and D10, such that D10 has the larger Zener voltage of the two, this guarantees that the transient voltage source derived from V_{DD} will yield to the auxiliary winding when the converter starts up and begins regulating.

This primary biasing scheme avoids using a bipolar transistor as a high-voltage pass element to provide the transient bias derived from V_{DD}.

The primary V_{BIAS} supply needs only to be designed to supply a load current of 35 mA, enough to power the two GAM modules and the two GMR isolators, and perhaps some additional low power housekeeping circuitry.

The drive signals to control the various power switches have to be carefully derived and timed in order to prevent incorrect switch assertions in time which can destroy the power switches. Also, proper delay/"dead" times must be inserted to ensure that there are no dynamic overlapping switch closures or unintentional simultaneous switching events. The timing diagram shown in Figure 10 shows the required four switch closures in time with respect to a master PWM signal for the ACFC. To allow for throughput delay and switching time differences in the four switch control paths it is recommended that as a starting point that the delay times added should be in the 25-50ns range for td1 and td4, the 100-125 ns range for td2 and td5, and the 150-175 ns range for td3 and td6. The result will be four signals that do not overlap except where the overlap is intentional and required: Between the primary power switch and the control output switch and between the clamp switch and the synchronous output switch.

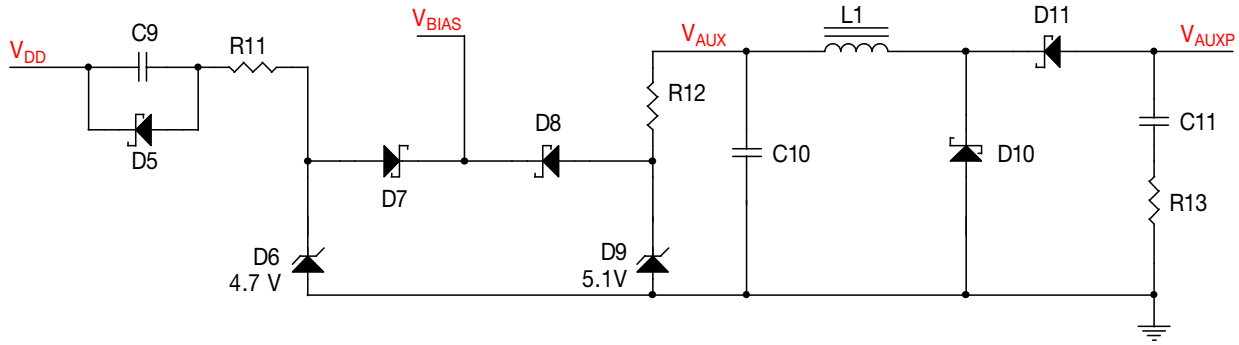


Figure 9. ACFC Primary Bias Circuitry

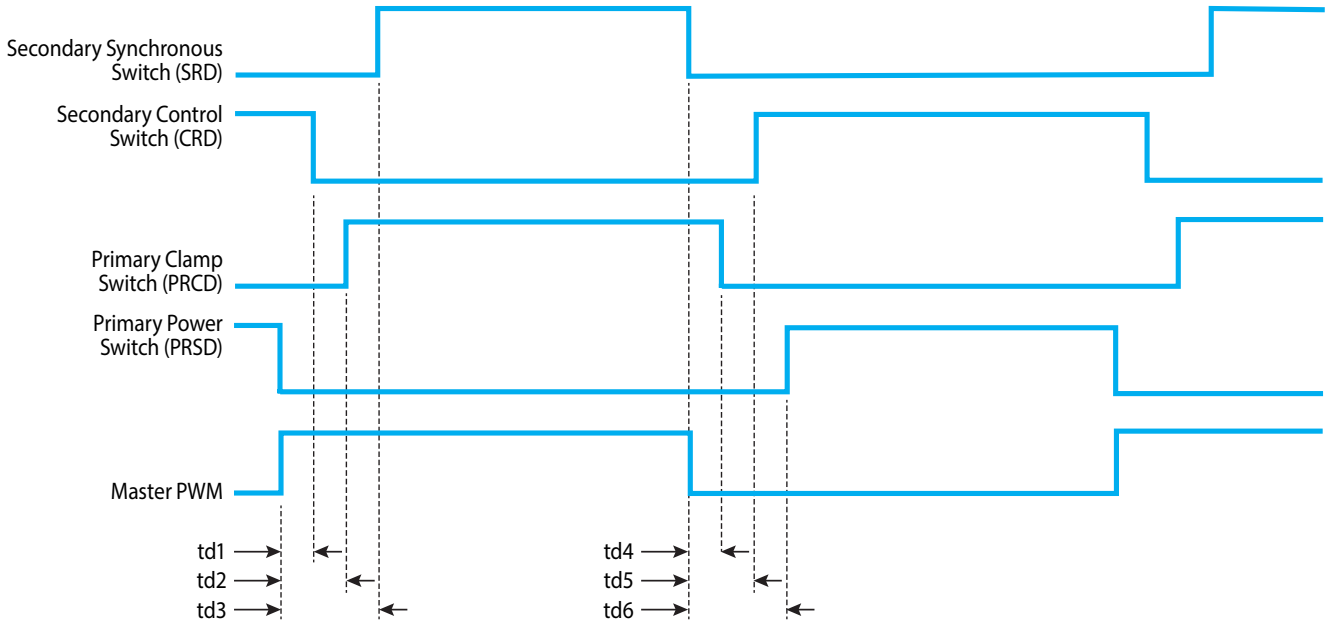


Figure 10. Power Switch Timing Relationships for the ACFC

Generating the requisite timing may be readily accomplished in code in firmware in a logic array device or microcontroller, or even with a handful of discrete components, as shown in Figure 11. During prototyping the delay times can be adjusted using R14 through R21 and C12 through C15 to obtain maximum efficiency with adequate switching margins.

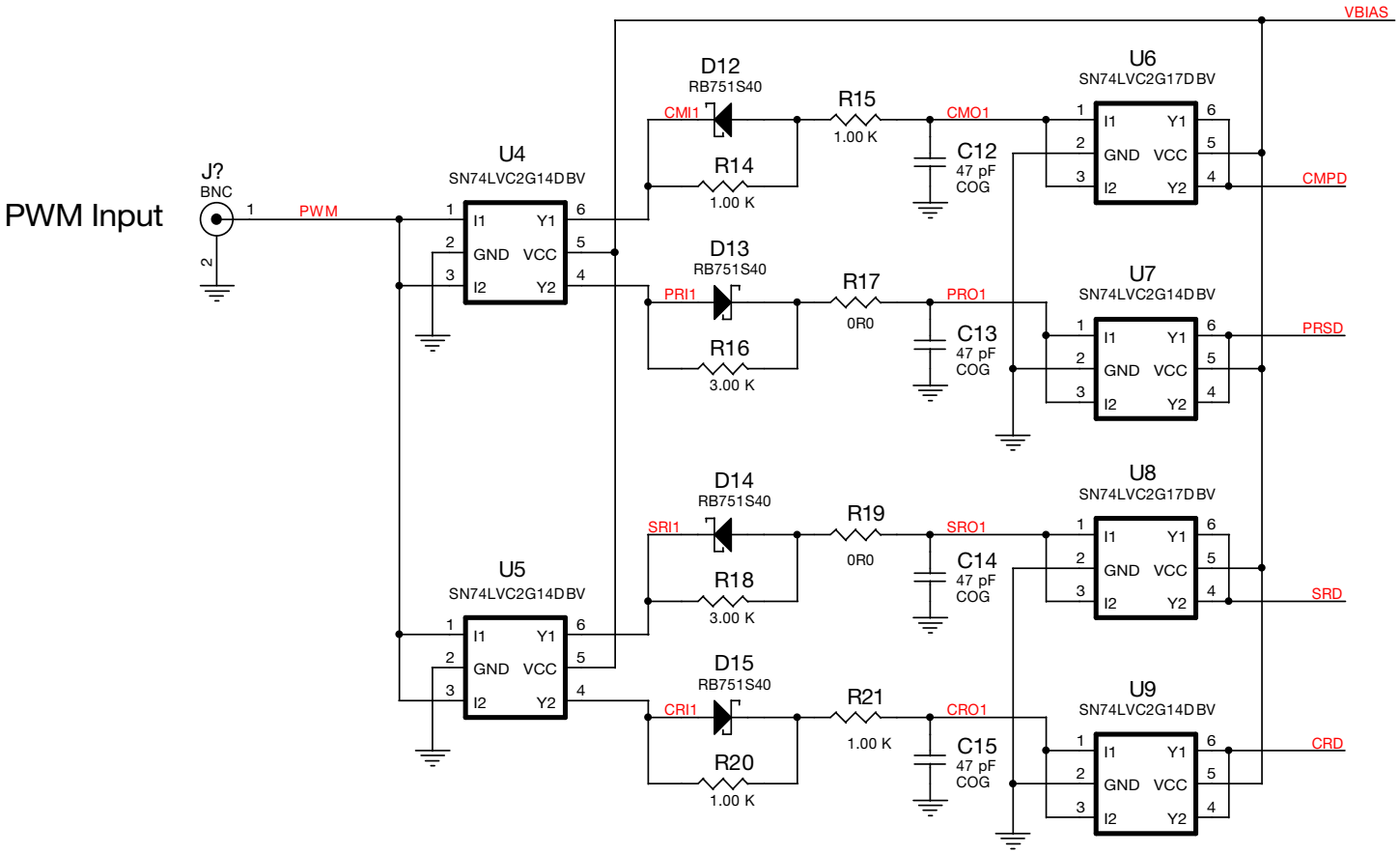


Figure 11. Discrete Component Delay and Dead Time Generation Circuit

SUMMARY

The forward power converter topology and its variants are discussed and the drawbacks of this converter topology are examined. The active-clamp forward converter is introduced and offered as the remedy to these drawbacks as it possesses all the benefits of the conventional forward converter (high efficiency and low parts count) while offering constrained power switch voltage stress during the power transformer's reset, as well as efficient recovery of the transformer reset energy along. A low parts-count example circuit is provided which utilizes four different modular and discrete products from the EPC Space product portfolio – FBS-GAM01, FBS-GAM04, FBS-GAM01-PSE modules and the FBG10N05 or the FBG20N04 discrete packaged HEMTs, along with GMR high-speed digital isolators, magnetic components, CMOS integrated circuits (for timing and delays) and passive discrete components -- to implement the ACFC topology. The resultant circuit satisfies all the aforementioned performance goals along with presenting the resulting small PCB area required, another critical consideration for space-based applications.

The versatility of the EPC Space product line-up is demonstrated with the previous example. The components presently available from EPC Space can and do serve as the building blocks for much higher level and higher performance power circuits and systems. The limit to what may be done using these products exists only in the mind of the designer!